A SINGLE-CHIP CDS AND 16 BIT ADC CCD VIDEO PROCESSING ASIC

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ABSTRACT

We describe our development of a single-chip preamplifier, correlated double sampling, and 16-bit analogue-to-digital conversion video processing ASIC for CCD cameras for space applications. In designing electronics for the space environment, there are strong requirements to minimise size, mass, and power dissipation, and yet to work from just a small catalogue of high-reliability space-qualified components. These requirements place severe constraints upon the CCD camera designer, particularly in the area of the analogue video signal processing and digitisation electronics. The problems are amplified with the ever increasing aspirations of the space science community with the call for larger focal plane arrays of multiple CCDs, reading out at increasingly higher pixel readout rates, and through multiple CCD output amplifiers. We describe our development and the measured performance of a single-chip ASIC solution which is intended to meet the requirements of the CCD cameras in the suite of Solar remote-sensing instruments on NASA's STEREO mission.

1 - INTRODUCTION

One of the most challenging problems facing the designer of space-qualified CCD camera electronics lies in the video processing chain. With many applications now wishing to exploit the low-noise MHz-rate capabilities of current CCDs, the camera designer is confronted with the problem of finding high-speed, low-noise op-amps, analogue-switches and analogue-to-digital converters (ADCs) that are radiation tolerant, and that can be procured with the appropriate levels of high-reliability component screening and space qualification.

In 1999/2000, and having been selected to develop the CCD Cameras for NASA's STEREO/SECCHI instruments, we considered the possibility of up-screening one of the high-speed monolithic CCD video processor ICs that had emerged on the commercial market for document scanners and digital cameras. These new ICs appeared to offer an elegant low-power solution, and overcome many of the problems associated with high-speed analogue signal design using discrete components. However, there still remained a number of problems, particularly for use in space applications.

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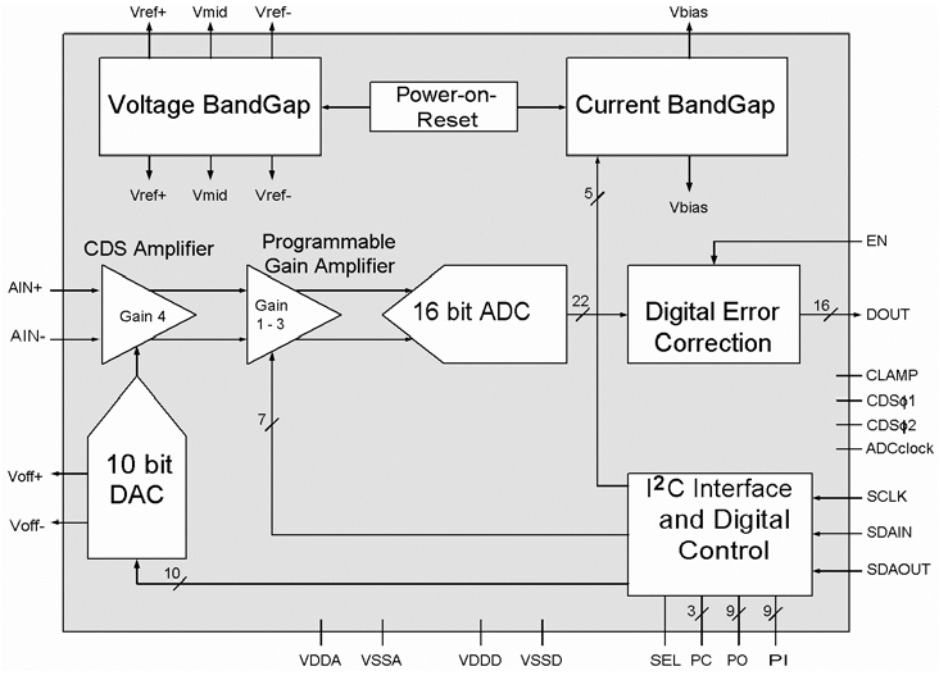
- Inadequate input-referred noise performance.
- Large (4 V) input signal range, thus still requiring a low-noise radiation-hard CCD preamplifier.
- Commercial temperature range plastic parts.
- Little or no data available concerning radiation tolerance.

Hence, and because we are fortunate to have an experienced group of mixed-signal ASIC designers within RAL's Microelectronics Group, we embarked upon a programme to develop our own science-grade CCD video processing ASIC for the STEREO/SECCHI cameras.

2 - THE CDS/ADC CCD VIDEO PROCESSING ASIC

A block diagram of the ASIC is shown in Figure 1 and the original requirement specifications are listed in Table 1.



A key feature of the design is the incorporation of a preamplifier with a signal gain of x4, thus eliminating the need for an external preamplifier. The CCD need only present a 1 V signal to achieve full swing in the ADC with unity gain set in the programmable gain amplifier. The preamplifier has differential inputs which, if connected appropriately, allow cancellation of any common-mode interference arising between the CCD and the ASIC. The inputs are AC-coupled from the CCD in order to isolate the ASIC from the typically high CCD output voltage pedestal. An internal pixel-rate clamp switch is used to restore the input signals to optimal bias values.

Correlated Double Sampling (CDS) is performed within the preamplifier circuitry using switched-capacitors. A schematic is shown in Figure 2. The design is again fully differential for enhanced rejection of common-mode noise and ground-bounce. A 10 bit DAC allows +/-500 mV of programmable DC offset to be introduced into the video signal. For the STEREO/SECCHI ASICs, now referred to as the "MK5" ASIC, the bandwidth of the preamplifier/CDS circuitry is optimized for a CCD readout rate of 1 Mpixels/s.

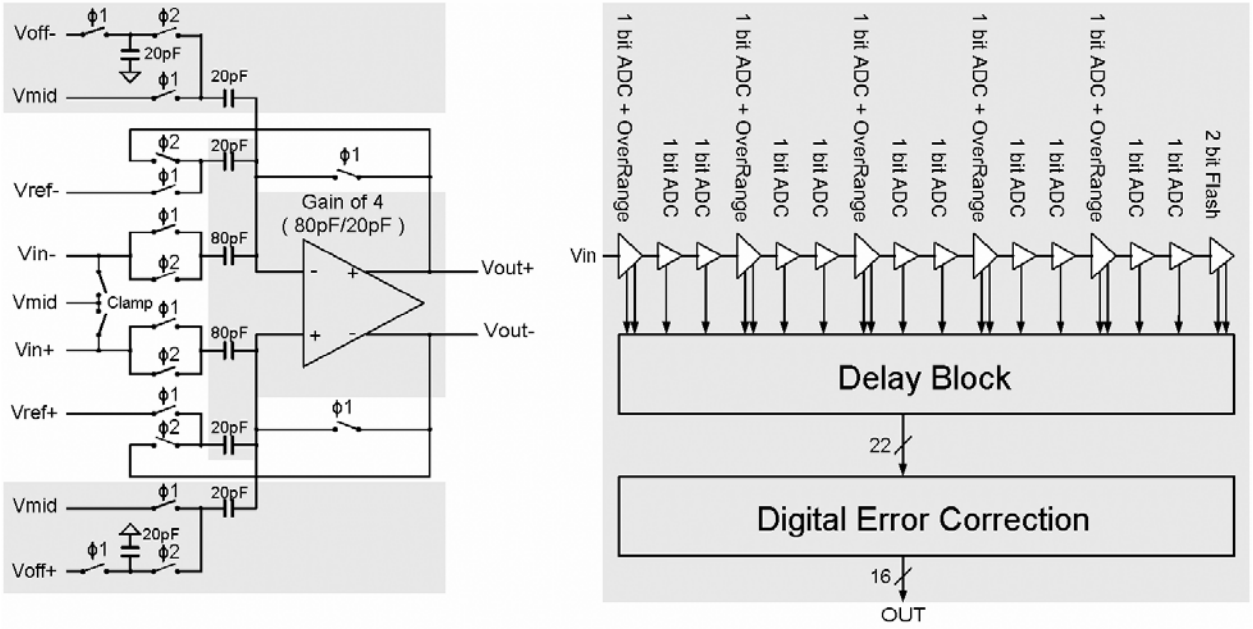


Figure 2 - Preamplifier/CDS and ADC

- DC Restoration of the CCD video signal.
- Fully differential-input preamplifier and CDS with 1 V video signal input range.
- Fully differential pipelined 16 bit ADC.
- Operation at up to at least 1 Mpixels/s readout rate.
- 10 bit programmable offset (+/- 500 mV - before programmable video gain).
- 7 bit programmable gain (gain = x 1 to x 3).
- Integral on-chip voltage and current bandgap references.
- Input referred system noise ≤ 3 adu rms (16 bits).
- 3-wire serial interface to program video gain and offset.
- Single 3.3 V power supply.
- Target power consumption ≤ 400 mW.
- Fabrication on a radiation tolerant CMOS process - total-dose ionising radiation tolerance ≥ 20 kRad. Triple-voting logic in digital interface and DAC registers for enhanced SEU immunity.
- Temperature Range: -50°C to +50°C.
- Packaging in a 84-pin CQFP with 0.025 inch lead pitch.

Table 1. Original CDS/ADC Video Processor ASIC Specification Requirements

A 7 bit programmable gain amplifier with a gain of 1-3 enables the CCD output voltage swing to be matched to the signal input range of the ADC. The ADC is a 16 bit fully differential pipelined converter using feedback capacitor switching in the amplifier stages, and over-ranging at intervals in order to minimise differential non-linearity (DNL) due to capacitor mismatching and amplifier gain errors. A block diagram is shown in Figure 2. The codes generated by each pipeline stage are fed into a delay block to ensure that all data appears at the output on the same clock cycle. Digital error correction adjusts for amplifier and comparator offsets.

There are two band-gap references to generate the various bias voltages and the bias current required by the amplifiers and comparators. The bias points are connected to output pins to allow for external decoupling. The ASIC is programmed through an I^2C compatible serial interface, and triple-voting logic is employed to enhance the single-event upset (SEU) tolerance of the logic and registers.

The ASIC has been fabricated on an AMS 0.35 micron 3.3 V CMOS process, known for its excellent tolerance to ionizing radiation.

With the inputs connected to ground, the MK5 ASIC achieves an input-referred noise of 2.8 ADU rms in 16 bits, equating to an input-referred noise of 42 µV rms within the 1 V signal input range. Running an e2v technologies CCD42-40, the total system noise is found to be 3.5 ADU rms at the specified 1 Mpixels/s readout rate. The contributions to the total input-referred noise are roughly balanced between contributions from kT/C noise on the input sampling capacitors, the internal voltage reference, and the preamplifier's transistor noise.

A photograph of the ASIC assembled on a STEREO/SECCHI CCD Driver Card is reproduced in Figure 3. A typical test image obtained in the laboratory using an e2v technologies CCD42-40 is reproduced in Figure 4.

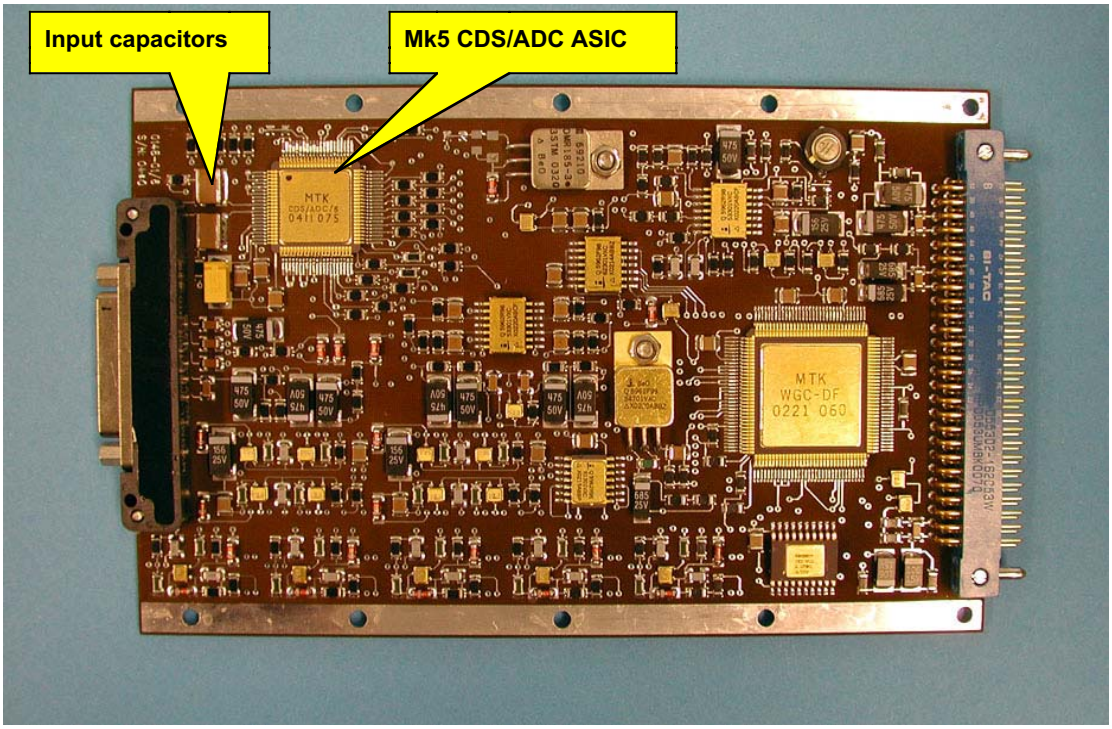


Figure 3 - STEREO/SECCHI PCB with MK5 CDS/ADC ASIC

A new version of the ASIC, the MK6, has been developed for the CCD Cameras on NASA's Solar Dynamics Observatory HMI and AIA instruments. The only difference between the MK5 and MK6 ASICs is that the internal bandwidth of the MK6 is optimized for a higher 2-2.5 Mpixels/s readout rate. The MK6 ASIC achieves an input-referred noise of 3.5 ADU rms in 16 bits, equating to an input-referred noise of 53 µV rms within the 1 V signal input range. Reading out an e2v technologies CCD42-40, the total system noise is found to be 4 ADU rms at 2 Mpixels/s.

Figure 4 - Test image from an e2v technologies CCD42-40 2k x 2k pixel CCD

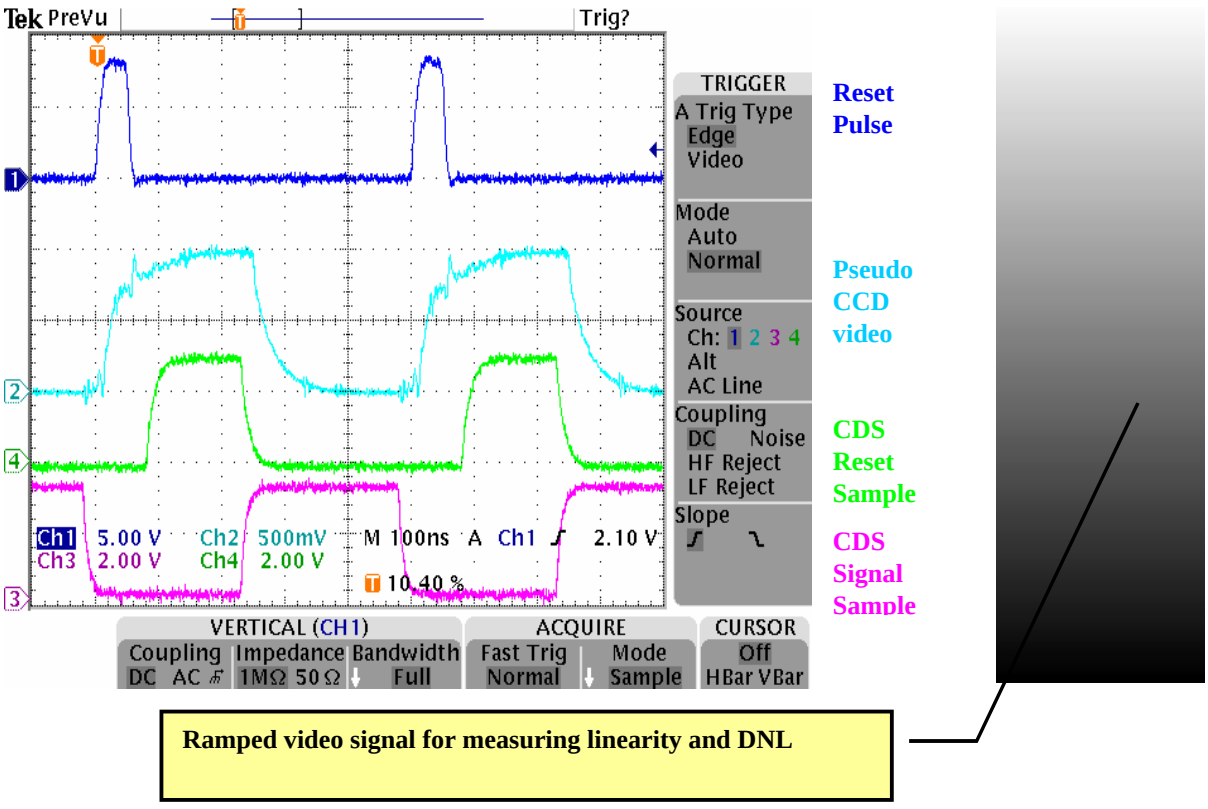


Figure 5 - ASIC Characterisation

The MK6 has recently undergone extensive laboratory testing. A programmable analogue waveform pattern generator was specially designed to generate pseudo CCD video waveforms to 16 bit precision. This was used to characterise the ASIC's overall linearity (INL), differential non-linearity, and dynamic response. Figure 5 illustrates the typical timing pulses recorded for a 2 Mpixels/s readout in which the waveform pattern generator was used to stimulate the ASIC with a "ramped" input response with each of the possible 16 bit (65,535 codes) being sampled 1000 times each. The measured INL is plotted in Figure 6 and the DNL in Figure 7.

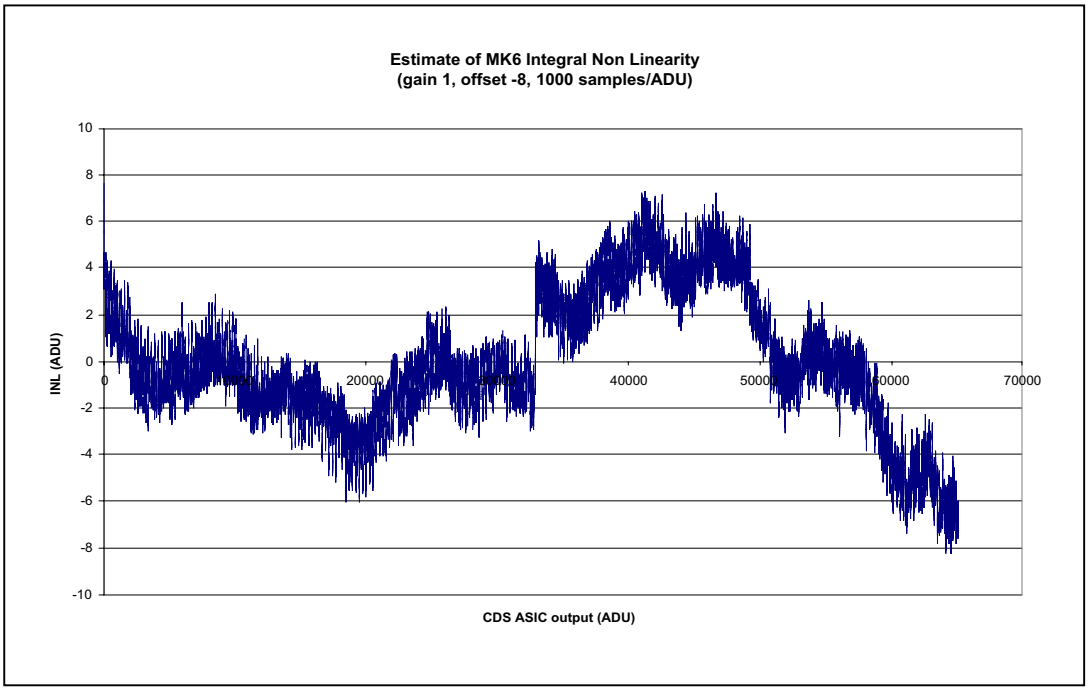


Figure 6 - INL – 16 bits

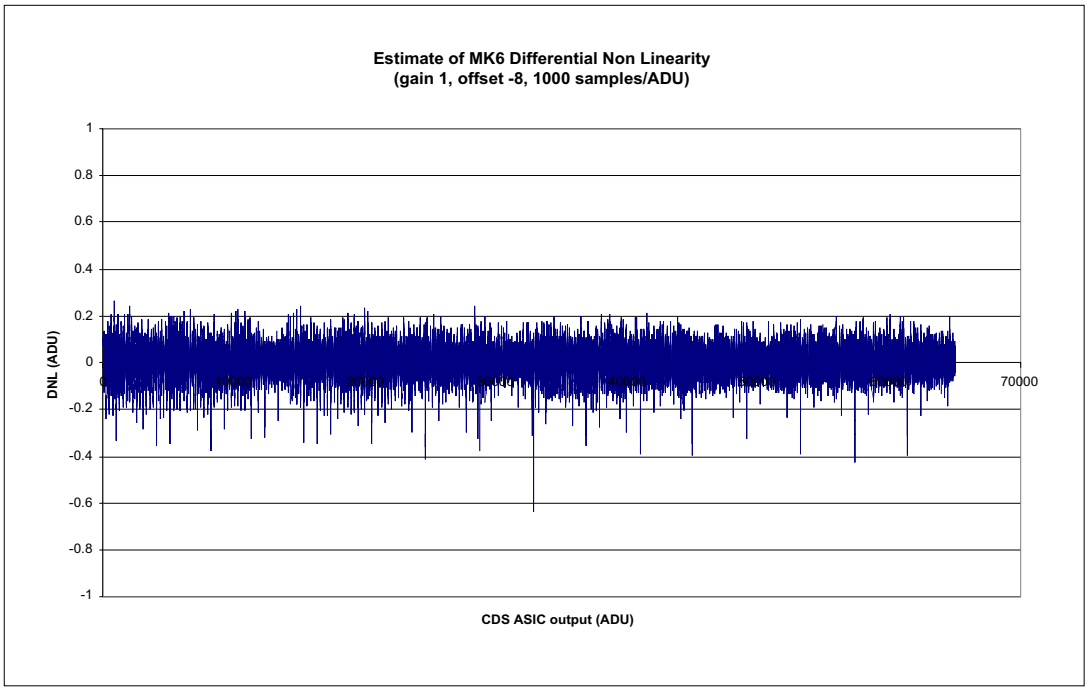


Figure 7 - DNL – 16 bits

In addition to the work at RAL, collaborators at the Mullard Space Science Laboratory (MSSL) have been characterising the ASIC's susceptibility to radiation damage using ESA test facilities. Heavy ion tests were performed at Louvain la Neuve in Belgium using Ne^{4+}, Ar^{8+} and Kr^{17+} ions at the Heavy Ion Facility. Total dose tests have been performed to 50 Krads at the Co^{60} source at ESTEC. The results are encouraging, but publication must await formal review and agreement with our collaborators.

The development programme for the ASIC is on-going, and a key objective is to reduce the overall input-referred noise. The current performance is ~ 14 bits, but our objective is to achieve 16 bits.

In the current MK5 design, the contributions to the total input-referred system noise are closely matched between three sources:

- kT/C noise on the input sampling capacitors.
- The internal voltage reference.
- The preamplifier's transistor noise.

The kT/C noise can be reduced by increasing the size of the input sampling capacitors at the cost of an increase in current consumption. However, this alone will not reduce the overall noise sufficiently. A redesign of the front-end preamplifier is required to reduce the contributions from transistor noise, and the noise-bandwidth of the on-chip voltage reference has to be reduced in proportion. Our perception is that these enhancements can be achieved with appropriate re-design, modelling and simulation.

In the longer term, we wish to reduce the operating power of the ASIC from the current value of 400 mW. A re-design of the 16 bit ADC will be required with a fundamental move away from the existing pipelined converter with its multiple amplifier stages.

Finally, we are also considering the possibility of transferring the design to a radiation-hard CMOS process that guarantees single-event latch-up immunity, i.e. a silicon-on-sapphire (SOS) or silicon-on-insulator (SOI) process.

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